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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,782	10/29/2001	Michael Yatziv	P4244 US/NP	5372

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EXAMINER	
VO, TIM T	
ART UNIT	**PAPER NUMBER**
2112	4

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

PR4

Office Action Summary	Application No. 10/002,782	Applicant(s) YATZIV, MICHAEL	
	Examiner Tim T. Vo	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 1-30 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:
A person shall be entitled to a patent unless --

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-30 are rejected under 35 U.S.C. § **102(b)** as being anticipated by Foth et al. patent number 5,867,648 referred hereinafter "Foth".

As for claims 1, 12, 16 and 28-30, Foth teaches a storage system, comprising: a host interface for receiving input/output ("I/O") transactions from a host device (see figure 1 and column 2 lines 48-61, wherein the figure 1 discloses a system 10 having connectivity for coupling to a client/server system to a mainframe system utilizing variety of bus protocol interfaces such as non-IBM, IBMPCMs, Server Net, SCSI, PCI, ISA, Fibre Channel, ATM, EISA, MCA, VME, S-BUS for connectivity (see column 2 lines 30-34), the I/O transactions complying with a first interface protocol (see column 2 lines 30-34); a storage device interface for transmitting I/O transactions to a plurality of storage devices according to a second interface protocol (see column 2 lines 30-34); and an interface adapter coupled to the host interface and the storage device interface (see

figure 1), wherein said interface adapter is configured to receive I/O transactions from the host interface, to convert the I/O transactions from the first interface protocol to the second interface protocol, and to transmit the converted I/O transactions to the storage device interface (see figures 1, 4A-4B, converter 18 , wherein the converter 18 converts different bus protocols such as non-IBM, IBMPCMs, Server Net, SCSI, PCI, ISA, Fibre Channel, ATM, EISA, MCA, VME, S-BUS), and the interface adapter is further configured to receive I/O transactions from the storage device interface, to convert the I/O transactions from the storage device interface from the second interface protocol to the first interface protocol, and to transmit the converted I/O transactions to the host interface (see figures 1, 4A-4B, converter 18 , wherein the converter 18 converts different bus protocols such as non-IBM, IBMPCMs, Server Net, SCSI, PCI, ISA, Fibre Channel, ATM, EISA, MCA, VME, S-BUS).

As for claims 2, 13 and 17, Foth teaches wherein: the second interface protocol is an IDE/ATA interface protocol (see column 2 lines 30-34).

As for claims 3, 14 and 18, Foth teaches wherein: the first interface protocol is a SCSI interface protocol (see column 2 lines 30-34).

As for claims 4, 15 and 19, Foth teaches wherein: the first interface protocol is a Fibre Channel interface protocol (see column 2 lines 30-34).

As for claims 5 and 20, Foth teaches wherein: the interface adapter is configured to receive a first plurality of frames corresponding to an I/O transaction generated by the host device (see figure 4A-4B and column 5 lines 11-52), wherein said interface adapter is configured to convert said first plurality of frames into a plurality of register inputs and

a command input corresponding to said I/O transaction, wherein said interface adapter is configured to cause said plurality of register inputs to be loaded into a plurality of registers on one of said plurality of storage devices, and wherein said interface adapter is configured to cause said command input to be loaded into a command register on said one of said plurality of storage devices (see figure 4A-4B and column 6 line 25 to column 7 line 59).

As for claims 6 and 21, Foth teaches, wherein said first plurality of frames arrive at said interface adapter in a serial format, and wherein said interface adapter is configured to deserialize said first plurality of frames (see figure 4A-4B and column 6 line 25 to column 7 line 59).

As for claims 7 and 22, Foth teaches wherein: the interface adapter includes a first receive buffer and a first transmit buffer coupled to the host interface, and said interface adapter further includes a second receive buffer and a second transmit buffer coupled to the storage device interface, wherein said first plurality of frames is received in said first receive buffer, and wherein said plurality of register inputs is received in said second transmit buffer prior to being loaded into said plurality of registers (see figure 4A-4B and column 6 line 25 to column 7 line 59).

As for claims 8 and 23, Foth teaches wherein: the interface adapter is configured to receive a plurality of register outputs from the storage device interface, convert said plurality of register outputs to a second plurality of frames, and convey said second plurality of frames to said host interface (see figure 4A-4B and column 6 line 25 to column 7 line 59).

As for claims 9 and 25, Foth teaches wherein: the interface adapter includes a state machine configured to receive a plurality of frames corresponding to an I/O transaction from said host interface, wherein said state machine is configured to convert said plurality of frames into a plurality of register inputs and a command input corresponding to said I/O transaction, wherein said state machine is configured to cause said plurality of register inputs to be loaded into a plurality of registers on one of the plurality of storage devices, and wherein said state machine is configured to cause said command input to be loaded into a command register on said one of the plurality of storage devices (see figure 4A-4B, 6-11 and column 6 line 25 to column 7 line 59).

As for claims 10 and 26, Foth teaches wherein the plurality of frames arrive at said state machine in a serial format, and wherein said state machine is configured to deserialize said plurality of frames (see figure 4A-4B and column 6 line 25 to column 7 line 59).

As for claims 11 and 27, Foth teaches a first receive buffer coupled to said host interface; a first transmit buffer coupled to said host interface; a second receive buffer coupled to said storage device interface; and a second transmit buffer coupled to said storage device interface; wherein said plurality of frames is received in said first receive buffer, and said plurality of register inputs is received in said second transmit buffer prior to being loaded into said plurality of registers (see figure 4A-4B and column 6 line 25 to column 7 line 59).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tim T. Vo
Primary Examiner
Art Unit 2112

4/17/04